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(54) Reliable interconnects with low via/contact resistance

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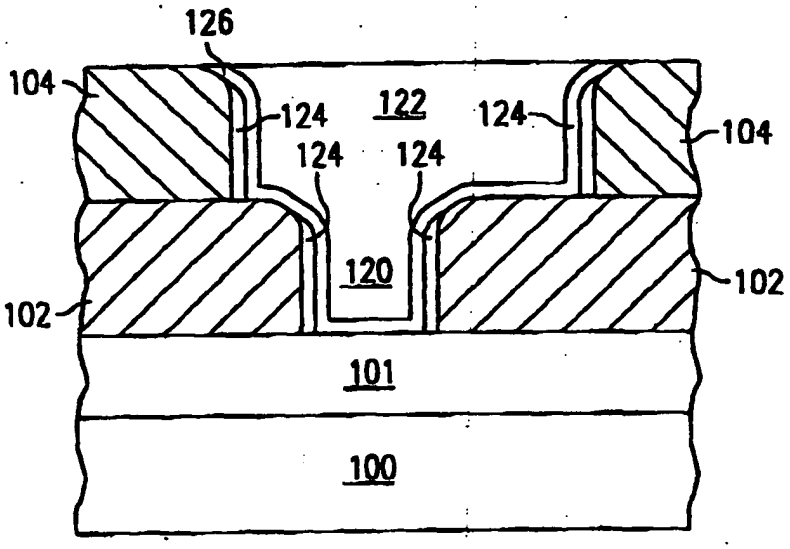

FIG. 2

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EUROPEAN SEARCH REPORT

Application Number
EP 02 10 0138

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 6 156 648 A (HUANG YIMIN) 5 December 2000 (2000-12-05) * column 2, line 7 - column 4, line 14; figures 2A-2F *	1-4,10, 11,13	H01L21/768
A	* the whole document *	5-9,12, 14,15	
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A	* the whole document *	9-11	
Y	US 6 177 347 B1 (LIU CHUNG-SHI ET AL) 23 January 2001 (2001-01-23) * column 2, line 50 - column 5, line 53; figures 5,6 *	1-8, 12-15	
A	* the whole document *	9-11	
A	US 5 933 753 A (SIMON ANDREW H ET AL) 3 August 1999 (1999-08-03) * column 3, line 25 - column 6, line 12; figures 3,4 *	1-4,7,8, 13-15	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 March 2003	Hedouin, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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& : member of the same patent family, corresponding document

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 10 0138

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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05-03-2003

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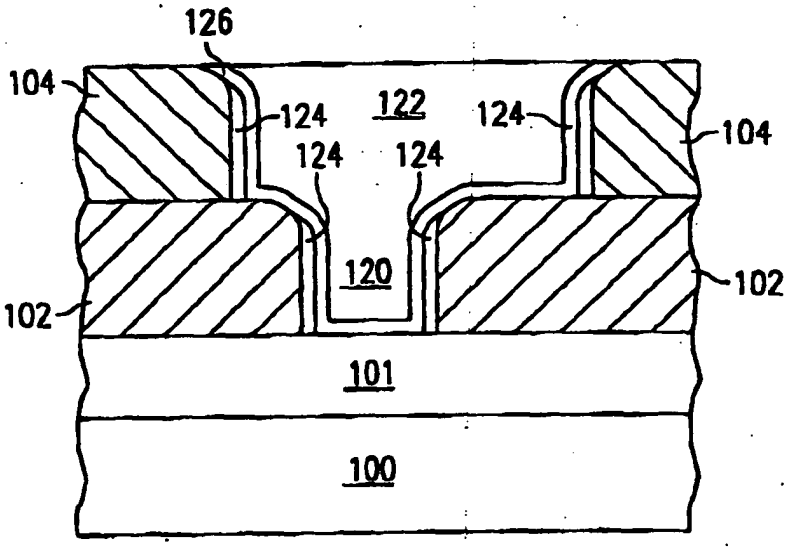

FIG. 2

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Description

FIELD OF THE INVENTION

[0001] The invention is generally related to the field of fabricating liners/barriers in contacts, vias, and copper interconnects in semiconductor devices and more specifically to the elimination of overhang in liner/barrier/seed deposition using sputter etch.

BACKGROUND OF THE INVENTION

[0002] As the density of semiconductor devices increases, the demands on interconnect layers for connecting the semiconductor devices to each other also increases. Therefore, there is a desire to switch from the traditional aluminum metal interconnects to copper interconnects. Unfortunately, suitable copper etches for a semiconductor fabrication environment are not readily available. To overcome the copper etch problem, damascene processes have been developed.

[0003] In a conventional interconnect process, the aluminum (and any liner/barrier metals) are deposited, patterned, and etched to form the interconnect lines. Then, an interlevel dielectric (ILD) is deposited and planarized. In a damascene process, the ILD is formed first. The ILD is then patterned and etched. A thin liner/barrier material is then deposited over the structure followed by copper deposition over the liner/barrier material. Then, the copper and liner/barrier material are chemically-mechanically polished to remove the material from over the ILD, leaving metal interconnect lines. A metal etch is thereby avoided.

[0004] The most practical technique for forming copper interconnects is electrochemical deposition (ECD). In this process, after the liner/barrier material is deposited, a seed layer of copper is deposited. Then, ECD is used to deposit copper over the seed layer. Unfortunately, physical vapor deposition (PVD) processes typically used to deposit the liner/barrier and seed materials have poor step coverage. This is due to the fact that PVD processes use a line of sight technique. As a result, an overhang 18 of liner/barrier 14 and/or seed 16 material occurs at the top of a trench or via 12 as illustrated in FIG. 1. The overhang causes a severe problem during the subsequent copper ECD. Specifically, a seam occurs in the copper fill material.

[0005] One proposed solution for overcoming the above problem uses a pre-sputter etch after the trench and via or contact etch, but before liner/barrier deposition. Unfortunately, the sputter etch step can deposit copper onto the sidewalls. Copper can then diffuse through the dielectric and cause reliability problems.

SUMMARY OF THE INVENTION

[0006] The invention uses a two layer barrier for a via or contact. A thin CVD barrier is deposited over a structure including within a via or contact hole. A sputter etch is then performed to remove the CVD barrier at the bottom of the via/contact. A second barrier is deposited after the sputter etch. A metal fill process can then be performed.

[0007] The invention provides an improved interconnect process having low via/contact resistance and improved reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the present invention, reference is now made to the following detailed description of certain particular and illustrative embodiments and the features and aspects thereof, by way of example only, and with reference to the figures of the accompanying drawings in which:

FIG. 1 is a cross-sectional view of a prior art liner/barrier/seed process that results in an overhang of material at the top of a trench, via, or contact;
FIG. 2 is a cross-sectional diagram of a via structure formed according to the first embodiment of the invention;
FIGs. 3A-3F are cross-sectional drawings of a copper interconnect structure formed according to the first embodiment of the invention; and
FIGs. 4A-4B are cross-sectional drawings of a contact structure formed according to a second embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0009] The invention will now be discussed with reference to forming vias in a copper damascene process. It will be apparent to those of ordinary skill in the art that the invention may also be applied to contact formation and to other metal interconnect processes.

[0010] A via structure 120 formed according to a first embodiment of the invention is shown in FIG. 2. Via structure 120 extends through an interlevel dielectric (ILD) 102 and connects between a lower copper interconnect 101 and an upper copper interconnect (trench structure 122). Via structure 120 comprises a first barrier/liner 124 located on the sidewalls of the via. First barrier/liner 124 does not extend along the bottom surface of the via. The thickness of first barrier/liner 124 may be in the range of 25-200Å.

[0011] Because first barrier/liner 124 does not extend along the bottom surface of the via, the resistivity of the material used for first barrier/liner 124 is not critical. Accordingly, a wider choice of materials is available. A material having good adhesion properties and good barrier properties against copper diffusion should be selected. For example, amorphous ternary transition metal-silicon nitrides such as TaSiN, TiSiN, MoSiN or WSiN may be used even though they typically have higher resistivity. Dielectrics, such as SiN may also be used. The pre-

ferred embodiment uses TiSiN deposited by CVD. CVD TiSiN offers excellent adhesion and barrier properties. Copper doesn't diffuse through TiSiN and the silicon bonds easily with the copper at the interface, resulting in good adhesion property.

[0012] Second barrier/liner 126 is located adjacent the first barrier liner 124 on the sidewalls of the via. Second barrier liner 126 does extend along the bottom surface of the via. Accordingly, the resistivity of the second barrier/liner 126 is important. In a preferred embodiment, second barrier liner 126 comprises a lower resistivity material than first barrier/liner 124. For example, PVD transition metals (such as Ta, Ti, Mo and W) or their nitrides such as TaN, TiN, WN, and MoN may be used. The thickness of second barrier/liner 126 is less than the thickness of prior art PVD barrier/liners. For example, the thickness may be in the range of 25-150Å. This layer is needed to make sure Cu has good adhesion on the upper surface (the first barrier/liner is removed from the upper surface, as will be discussed below).

[0013] A method for forming the via structure 120 of FIG. 2 will now be discussed with reference to FIGs. 3A-3F. A semiconductor body 100 is processed through formation of trench and vias in a metal interconnect level, as shown in FIG. 3A. Semiconductor body 100 typically comprises a silicon substrate with transistors and other devices formed therein. Semiconductor body 100 also includes the pre-metal dielectric (PMD) and may include one or more metal interconnect layers. Only copper interconnect 101 is shown.

[0014] An ILD (interlevel dielectric) 102 is formed over semiconductor body 100 (including copper interconnect 101). IMD (intrametal dielectric) 104 is formed over ILD 102. An etchstop layer (not shown) may optionally be placed between ILD 102 and IMD 104. Suitable dielectrics for ILD 102 and IMD 104, such as silicon dioxides, fluorine-doped silicate glass (FSG), organo-silicate glass (OSG), hydrogen silesquioxane (HSQ), and combinations thereof, are known in the art. ILD 102 and IMD 104 are thick dielectric layers having a thickness in the range of 0.1 um - 1 um.

[0015] In a copper dual damascene process, both the vias and trenches are etched in the dielectric. Via 106 is etched in ILD 102 and trench 108 is etched in IMD 104. Via 106 is used to connect to underlying metal interconnect layer 101. Trench 108 is used to form the metal interconnect lines.

[0016] First barrier/liner layer 124 is deposited using a CVD process over IMD 104 including in trench 108 and via 106, as shown in FIG. 3B. CVD allows a thin conformal layer to be deposited. The thickness of first barrier/liner 124 may be in the range of 25 -200Å.

[0017] Referring to FIG. 3C, a sputter etch is then performed. An inert gas with or without H2, such as Ar, H_2/N_2, or H_2/Ar. Argon sputtering, is used in the preferred embodiment. Sputter etching uses a line-of-sight that removes more material on the horizontal surfaces than on the vertical surfaces. Accordingly, the portions of first barrier/liner 124 on the upper surface of IMD 104, the bottom of trench 108, and the bottom of via 106 are removed. The upper corners of via 106 and trench 108 are both also pulled back.

[0018] Sputter-etching at the via bottom functions to breakthrough the barrier 124 and clean the via bottom. Because this exposes the copper from the underlying copper interconnect 101, some copper is sputtered onto the sidewalls of the via. However, the first barrier/liner 124 prevents this copper from diffusing into the dielectric and causing reliability problems.

[0019] Because first barrier/liner 124 is removed at the bottom of the via, the resistivity of the material used for first barrier/liner 124 is not critical. A material having good adhesion properties and good barrier properties against copper diffusion should be selected. For example, amorphous ternary transition metal-silicon-nitrides such as TaSiN, TiSiN or WSiN may be used even though they typically have higher resistivity. Dielectrics, such as SiN may also be used. The preferred embodiment uses TiSiN. CVD TiSiN offers excellent adhesion and barrier properties. Copper doesn't diffuse through TiSiN and the silicon bonds easily with the copper at the Cu-barrier interface.

[0020] After the sputter etch, the second barrier/liner layer 126 is deposited, as shown in FIG. 3D. Either PVD or CVD may be used. The thickness of second barrier/liner layer 126 may be in the range of 25 -150Å. Because a thin layer is deposited and the top corners of the via and trench are both pulled back during the sputter etch, the overhang of the PVD barrier is not an issue. However, since the second barrier/liner 126 remains at the bottom of the via (i.e., in the electrical path), the resistivity of the second barrier/liner 126 is important. Accordingly, a PVD or CVD process with transition metal or its nitride such as Ta, Ti, Mo, W, TaN, TiN, WN, and MoN may be used.

[0021] In a copper electro-chemical deposition (ECD) process, a copper seed layer is deposited over the second barrier/liner layer 126. The seed layer is typically deposited using a PVD process. Copper ECD is then performed as shown in FIG. 3E to form copper layer 118. Various copper ECD processes are known in the art. In one example, a 3-step process is used. After placing the wafer in the plating solution, a current of approximately 0.75 Amps is passed through the seed layer for a time on the order of 15 secs. The current is then increased to around 3 Amps for approximately 60 seconds. Final plating occurs at a current of about 7.5Amps with the duration determined by the final desired thickness. A quick spin-rinse dry (SRD) is performed in the plating cell above the plating solution. The wafer is then transferred to the SRD cell and a post-ECD SRD is used to clean the plating residue.

[0022] Processing then continues to chemically-mechanically polish (CMP) the copper layer 118 and second barrier/liner 126 to form the copper interconnect, as shown in FIG. 3F. An additional advantage of the inven-

tion is that the CMP is less difficult due to the thin second barrier/liner 126. A thicker barrier is more difficult to CMP. Additional metal interconnect layers may then be formed followed by packaging.

[0023] A second embodiment of the invention will now be discussed with reference to FIGs. 4A-4B. As in the first embodiment, a semiconductor body 100 is processed through formation of trench 108 and vias 106 in a metal interconnect level. Then, as shown in FIG. 4A a PVD barrier layer 224 is first deposited over the structure including within the trench 108 and via 106. A thickness on the order of 250Å is used. Since the PVD deposited barrier will remain at the bottom of the via, a low resistivity material is used. For example, ternary transition metal nitride may be used.

[0024] Next, a CVD barrier layer 226 is deposited over the PVD barrier 224.The CVD barrier layer 226 has a thickness in the range of 25-100Å. Because the CVD barrier 226 will be removed at the bottom of the via, resistivity of the material is not critical. A material having good adhesion properties and good barrier properties against copper diffusion should be selected. For example, amorphous ternary transition metal-silicon-nitrides such as TaSiN, TiSiN or WSiN may be used even though the typically have higher resistivity. Dielectrics, such as SiN may also be used. The preferred embodiment uses TiSiN deposited by CVD.

[0025] After both barrier layer have been deposited, a sputter etch is performed, as shown in FIG. 4B. An inert gas, such as argon, may be used. The sputter-etch is tuned to remove portions of CVD barrier layer 226 at the bottom of via 106 as well as on the other horizontal surfaces. During this step, the top corners of the trenches and vias are also pulled back to eliminate the overhang that is created during the PVD barrier process (layer 224).

[0026] Processing then continues with the deposition of the copper seed layer and copper fill process. The second embodiment is less preferred than the first embodiment. The sputter etch of the second embodiment is difficult to control.

[0027] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. For example, the invention may be applied to forming contacts instead of vias.

[0028] Another alternative embodiment of the method of the present invention might comprise: forming a dielectric layer over a semiconductor body; forming a hole in said dielectric layer; depositing a first barrier layer over said dielectric layer including in said hole using physical vapour deposition; depositing a second barrier layer over said first barrier layer using chemical vapour deposition; performing a sputter etch to remove said second barrier layer from a bottom of said hole; and filling said hole with a metal. The second barrier layer may comprise silicon nitride or a transition metal-silicon-nitride, and the first barrier layer may comprise a transition metal-nitride.

Claims

1. A method of fabricating an integrated circuit comprising:

   forming a dielectric layer over a semiconductor body;
   forming a hole in said dielectric layer;
   depositing a first barrier layer over said dielectric layer including in said hole using chemical vapor deposition;
   performing a sputter etch to remove said first barrier layer from a bottom of said hole;
   depositing a second barrier layer over said first barrier layer and said dielectric layer; and
   filling said hole with a metal.

2. The method of claim 1, wherein said hole comprises a via.

3. The method of claim 1, wherein said hole comprises a contact.

4. The method of any preceding claim, wherein said metal comprises a material selected from the group consisting of: tungsten, aluminum, copper, or a combination thereof.

5. The method of any of claims 1-4, wherein said first barrier layer comprises a dielectric barrier material.

6. The method of any of claims 1-4, wherein said first barrier layer comprises a ternary transition metal-silicon-nitride.

7. The method of any of claims 1-6, wherein said second barrier layer comprises a material selected from the group consisting of: transition metals and transition metal nitrides.

8. The method of any of claims 1-6, wherein said second barrier layer comprises a material having lower resistivity that a material of the first barrier layer.

9. The method of any preceding claim, wherein the first barrier layer has a thickness in the range 25-200Å.

10. The method of any preceding claim, wherein the second barrier layer has a thickness in the range 25-150Å.

11. The method of any preceding claim, wherein said second barrier layer is deposited using physical vapor deposition.

12. The method of any preceding claim, wherein said second barrier layer is deposited using chemical vapor deposition.

13. An integrated circuit, comprising:

a dielectric layer;
a conductive structure embedded in said dielectric layer, wherein the conductive structure comprises:

a first barrier layer at the outer sidewalls of the conductive structure, the first barrier layer not extending along a bottom of said conductive structure;
a second barrier layer extending along the first barrier layer at the sidewalls and extending across the bottom of said conductive structure, the second barrier layer having a lower resistivity than the first barrier layer; and
a metal fill layer.

14. The integrated circuit of claim 13, wherein the first barrier layer comprises metal-silicon nitride.

15. The integrated circuit of claim 13 or claim 14, wherein the second barrier layer comprises a transition metal or transition metal-nitride.

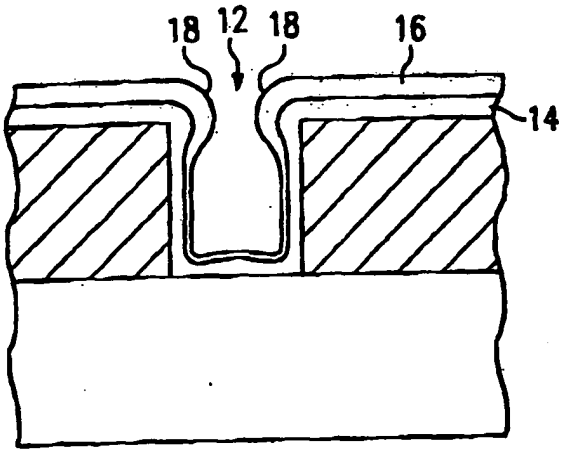

FIG. 1
(PRIOR ART)

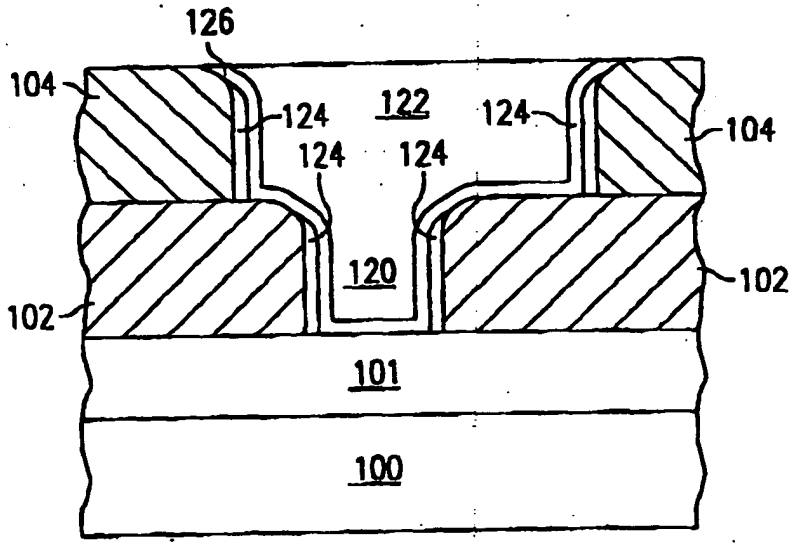

FIG. 2

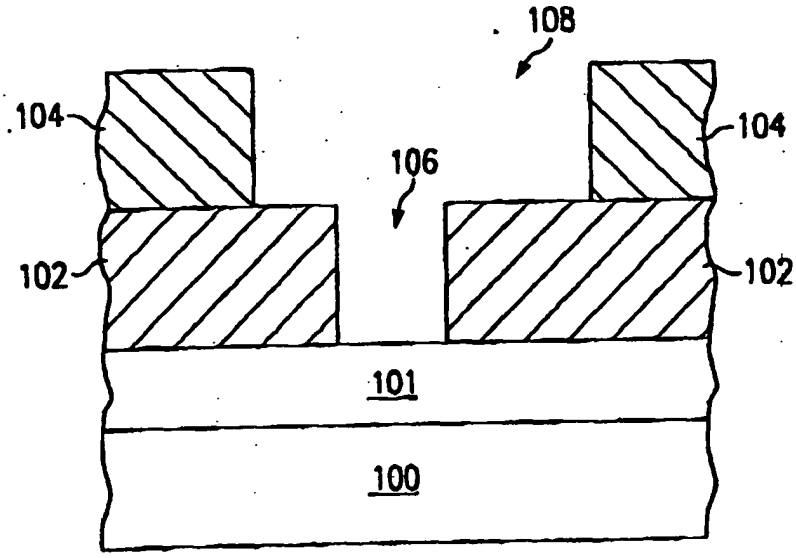

FIG. 3A

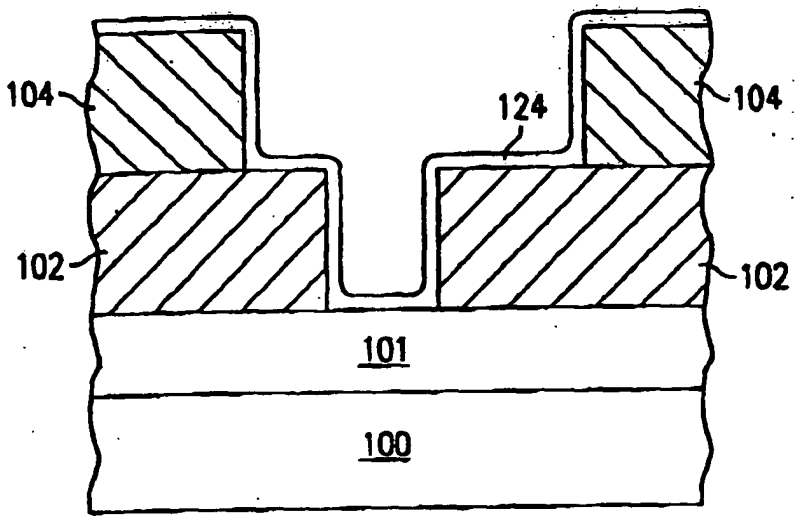

FIG. 3B

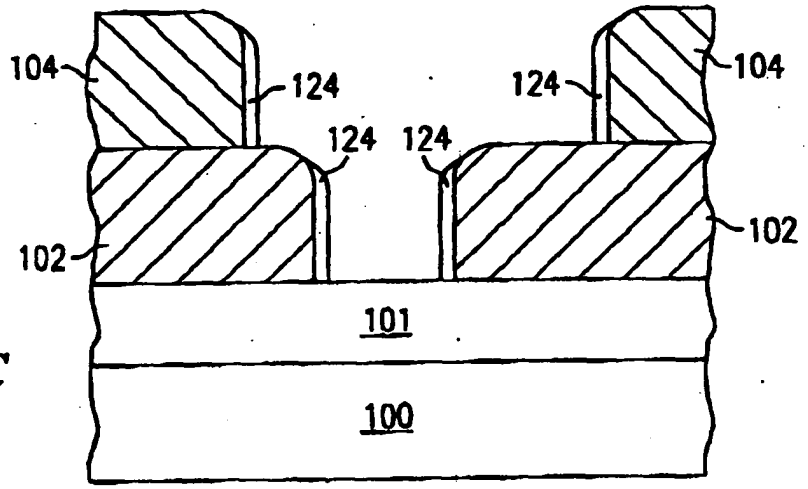

FIG. 3C

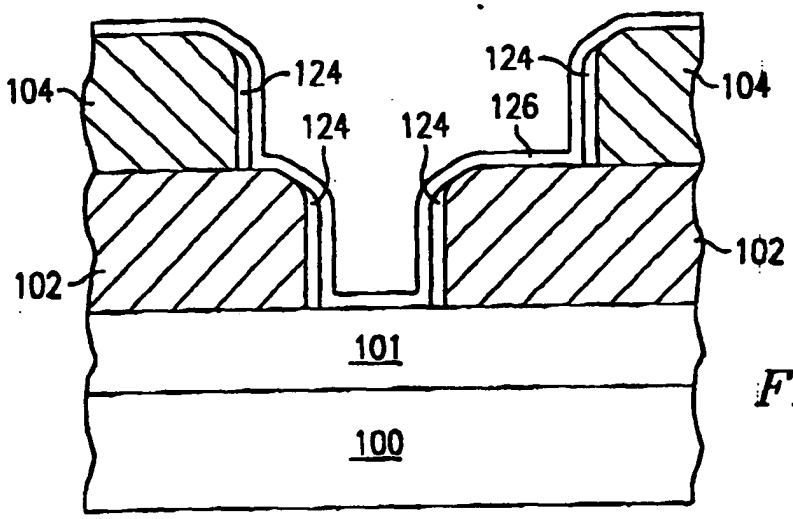

FIG. 3D

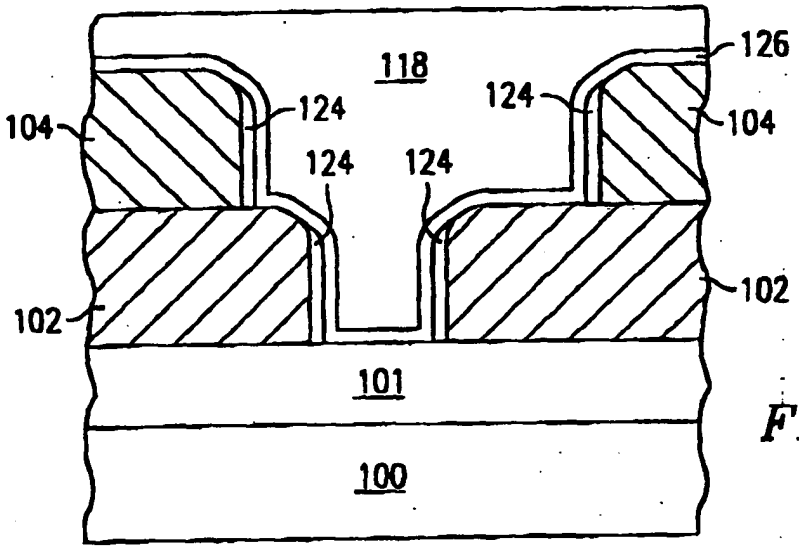
118
126
124
124
104
104
124
124
102
102
101
100

FIG. 3E

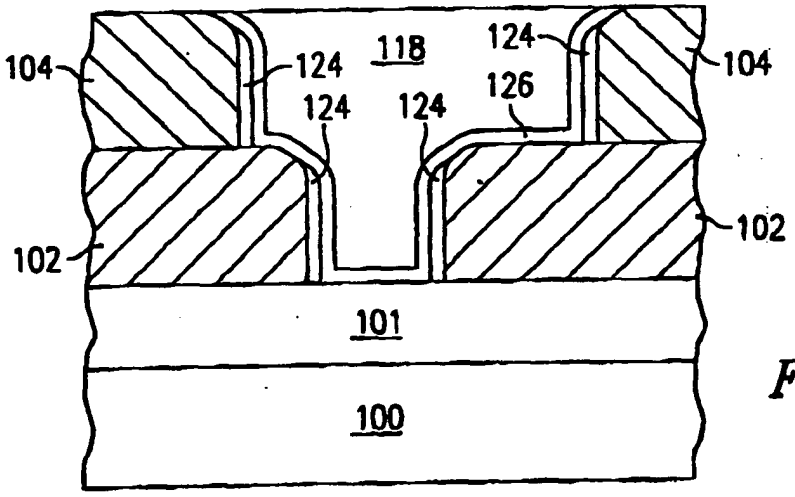
104
124
118
124
104
126
124
124
102
102
101
100

FIG. 3F

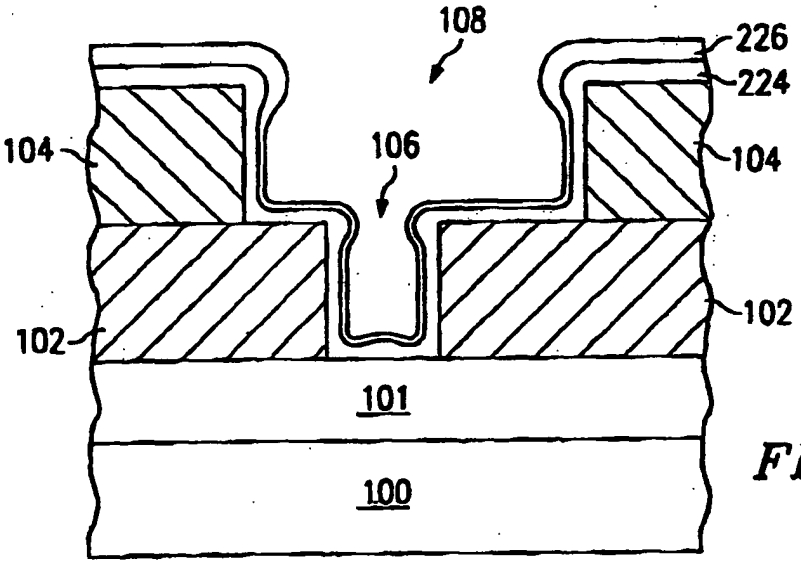
108
226
224
104
106
104
102
102
101
100

FIG. 4A

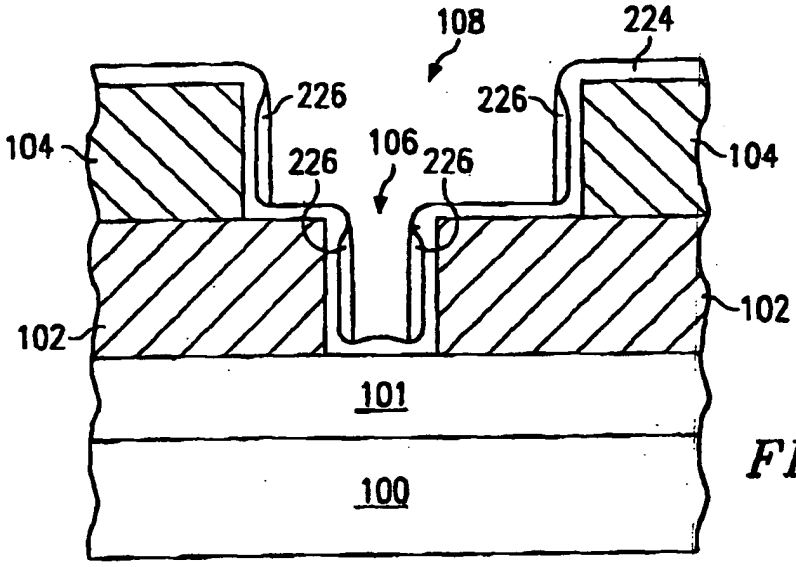
108
224
226
226
104
226
106
226
104
102
102
101
100

FIG. 4B